

UNITED STATES PATENT APPLICATION
for a new and useful invention entitled

LEADLESS CHIP CARRIER DESIGN AND STRUCTURE

by Inventor:

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BACKGROUND OF THE INVENTION

1. Field of the Invention

5 The present invention generally relates to electronic packaging, and more particularly, to a leadless chip carrier design and structure.

2. Description of the Related Art

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10 The microelectronics industry has continued to make significant advances in semiconductor device technology. Semiconductor devices are getting smaller, more dense, and run at higher speeds. However, as device sizes decrease and electrical components are moved closer together, one of the limiting properties of the semiconductor device is the electrical parasitics caused by resistance, capacitance and inductance effects. This is particularly troubling in radio frequency (RF) devices, where it is important to minimize electrical parasitics and to be able to predict their effects reliably. Also, the need to control device generated heat has become more critical as the speeds and power consumption of semiconductor devices has increased.

20 Controlling electrical parasitics is also important at the packaging level. The structure that supports the semiconductor device (i.e., chip) is commonly referred to as an electronic package. The electronic package is designed to provide electrical interconnection for I/O, signal lines, power supplies, and ground, in addition to environmental and physical protection.

25 One advantageous form of packaging is the chip carrier which is gaining in popularity. A big reason for this is that chip carriers are very small in size and thus make it possible to fit many devices on a substrate such as a printed circuit board (PCB) or ceramic. The package, as part of the completed semiconductor device, must be low in electrical parasitics and have good thermal dissipation. This is especially important for RF applications.

Electrical parasitics, particularly inductance, are some of the parameters that can adversely affect the performance of electrical packages. Inductance is thus one parameter that should be controlled and reduced. One of the factors contributing to the inductance is the long printed traces found in most packages. Another factor is the lack of a good ground plane located close to the device.

Present packages also have problems with dissipating heat. As semiconductor devices have increased in performance, their power requirements have also increased dramatically. Because of the large amount of power needed to operate a chip, the heat generated by a chip can reach several watts. Dissipation of this heat is an important design consideration of both the chip and chip carrier. Since the chip and chip carrier are made from different materials, each having a different coefficient of thermal expansion, they will react differently to the heat generated by the chip and the outside environment. The resulting thermal stresses can reduce the life of the semiconductor device by causing mechanical failures. Thus, it is desirable to be able to predict accurately the thermal effects of the chip carrier so that the chip carrier can be designed accordingly.

Therefore, there exists a need for a small package for a semiconductor device that would provide low electrical parasitics, predictable heat dissipation along with an efficient ground plane.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the present invention, a semiconductor device is provided in the form of a chip carrier that includes a semiconductor chip attached to the upper surface of an interconnect substrate. A die attach pad is provided on the upper surface of the interconnect substrate and the chip is attached to this pad. On the lower surface of the substrate is a heat spreader positioned beneath the die attach pad. A plurality of vias extend through the thickness of the substrate from the upper surface to the lower surface. A first group of these vias is positioned to intersect both the die attach pad and the heat spreader. A second group of these vias is positioned apart from both the die attach pad and the heat spreader. Bonding pads are positioned to abut the second group of vias on the upper surface

BRIEF DESCRIPTION OF THE DRAWINGS

A preferred embodiment of the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The preferred embodiment, however, both as to organization and method of operation, may best be understood by reference to the following description taken in conjunction with the claims and the accompanying drawings, in which like parts may be referred to by like numerals:

FIG. 1 illustrates an electronic packaging hierarchy;

FIGS. 2-4 illustrate, in cross-sectional, top and bottom views, respectively, one embodiment of the invention; and

FIG. 5 illustrates, in cross-section view, a chip carrier in accordance with an alternate embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

The present invention provides for a more efficient electronic device particularly suited for radio frequency (RF) applications by minimizing electrical parasitics and providing for predictable electrical and thermal performance. The electronic device in accordance with the invention is especially applicable to devices with up to approximately 64 leads, which is particularly suited to many RF and analog applications, but it will be readily appreciated that the following description also applies to packages of different sizes and different number of I/O pins.

Referring now to **FIG. 1**, an electronic packaging hierarchy is illustrated. A semiconductor device chip 100 is mounted on an electronic package 110 to form a semiconductor device 120. The resulting semiconductor device can be connected to a printed circuit board 130 that is plugged into a mother board (not shown).

FIG. 2 illustrates in cross-section, a semiconductor device 120 in accordance with a preferred embodiment of the present invention. Device 120 includes semiconductor device chip 100 which is preferably an integrated circuit (IC) chip. The semiconductor device also

includes an interconnect substrate 220 having an upper surface 200 and a lower surface 210. The upper and lower surface of the interconnect substrate preferably are planar. Upper surface 200 of the interconnect substrate has a die attach bond pad 240 to which semiconductor device chip 100 is attached. Die attach bond pad 240 is a metallic pad formed of a metal that is highly conductive, both electrically and thermally. In the preferred embodiment, interconnect substrate 220 suitably comprises an organic (i.e., laminate) material such as a polytetrafluoroethylene (PTFE) or FR4 based laminate. However, other alternative embodiments may use other organic or non-organic (i.e., ceramic) materials for interconnect substrate 220.

Semiconductor device chip 100 is attached to die attach bond pad 240 of interconnect substrate 220 using a conventional conductive epoxy die attach epoxy 230. For example, an epoxy such as Ablebond 84-ILMIT or Sumitomo 1079B can be used. Alternatively, solder or other well known die attach material can be used depending on the interconnect substrate material and the intended use of the device.

A heat spreader 290 is located on lower surface 210 of interconnect substrate 220. Similar to die attach bond pad 240, heat spreader 290 is a metallic pad formed of a metal that is highly conductive, both electrically and thermally. As described below, heat spreader 290 is used to both electrically and thermally connect semiconductor device 120 to a printed circuit board (PCB).

A plurality of vias passes through the thickness of interconnect substrate from upper surface 200 to lower surface 210. Each of the vias is filled with a material such as copper that is both electrically and thermally conductive. The filled vias thus provide electrical and thermal pathways from upper surface 200 to lower surface 210.

A first group of vias 255 are illustrated in FIG. 2. First group of vias 255 is positioned to intersect both die attach pad 240 on the upper surface and heat spreader 290 on the lower surface 210 of interconnect substrate 220. First group of vias 255 thus provides for a good thermal and electrical connection from semiconductor device chip 100 to heat spreader 290 due to the presence of an electrical and thermal conductor such as copper.

A second group of vias 250 is positioned about the periphery of and spaced away from semiconductor device chip 100 as is more clearly seen in FIG. 3. FIG. 3 illustrates semiconductor device 120 in top view. In accordance with the invention, a plurality of bond pads 260 is formed on upper surface 200 of interconnect substrate abutting the second group of vias 250. The plurality of bond pads is preferably positioned in a peripheral design along the perimeter of the upper surface of the interconnect substrate. However, it will be appreciated that the plurality of bond pads may be positioned in other designs such as either a regular or irregular array of columns and rows. Whatever the design, the second group of vias 250 and the array of bond pads 260 are designed so that the vias abut the pads.

Semiconductor device chip 100 includes a plurality of device electrodes 300 on its upper surface. These device electrodes 300 provide the means by which electrical contact, including I/O, power supplies, and ground, is made to the electrical circuit contained on semiconductor device chip 100. Electrical connection must be made from device electrodes 300 to bond pads 260 of interconnect substrate 220 and ultimately to the printed circuit board and the mother board.

Referring to FIGS. 2 and 3, in the preferred embodiment, semiconductor device chip 100 is electrically connected to interconnect substrate 220 of the chip carrier by a technique called wire bonding. In wire bonding, the electrical connections are made by bonding wires 270, preferably very small wires, between device electrodes 300 of the semiconductor device chip 100 to bond pads 260 on interconnect substrate 220. The bond attachment is completed by thermal compression bonding or other well known wire bonding methods. Typically, wires and bond pads that are gold or gold-plated, aluminum or an alloy of aluminum, or copper or an alloy of copper are used.

In accordance with the invention, as illustrated in FIG. 3, each of the plurality of bond pads 260 is located immediately adjacent to or abuts one of second group of vias ²⁵⁰~~260~~. No traces are necessary between the bond pads and the vias, so parasitic inductance is reduced. The bond pads 260 are directly coupled to the plurality of lands 280 located on the lower surface 210 of the interconnect substrate 220 by the copper or other conductive material filling the vias. The lands 280 can be connected to a signal on the PCB 130 or to a ground or power

source. It will be readily appreciated that this will reduce the electrical inductance of semiconductor device 120 as this minimizes the distance from bond pads 260 to vias 250. Thus, the flexibility of wire bonding can be utilized to pick the shortest path from semiconductor device chip 100 to bond pads 260 and the resultant inductance will be minimal.

5 Space is saved since traces are not needed to connect bond pads 260 to vias 250. It has been found, for example, that what was previously a 9x9 mm 48 I/O package can be reduced to a 6x6 mm 48 I/O package. Therefore, the size of interconnect substrate 220 is only slightly larger than the size of semiconductor device chip 100.

Referring now to **FIG. 4**, a bottom view of semiconductor device 120 according to a preferred embodiment of the present invention is illustrated. Second group of vias 250 passes through interconnect substrate 220 and are exposed on lower surface 210. Lower surface 210 of the interconnect substrate 220 also has a plurality of lands 280 and heat spreader 290. Lower surface 210 of interconnect substrate 220 is adapted to be attached to the printed circuit board (not shown) by soldering heat spreader 290 and plurality of lands 280 to corresponding metallization on the printed circuit board. Using heat spreader 290 to attach to the printed circuit board allows for a good thermal path at a very low thermal resistance. Large heat spreader 290 also helps to increase the reliability of the bonds to the plurality of lands 280 as is explained below.

There is increased reliability because the mechanical stress or physical displacement on the plurality of lands 280, due to the heating and cooling of the semiconductor device, is decreased due to the presence of large heat spreader 290. A difference may exist in the coefficient of thermal expansion (CTE) between the semiconductor device and the PCB because they may be constructed of different materials. If so, when the semiconductor device heats up due to operating or environmental factors, there will be a physical strain on the connections (i.e., lands 280 and heat spreader 290) between the semiconductor device and the PCB to which the semiconductor device is attached. The copper exposed pad of large heat spreader 290 reduces the CTE mismatch. The large exposed pad of heat spreader 290 more than compensates for the 4-6 mil nominal solder stand-off between the semiconductor device

and the PCB. Heat spreader 290 dominates the overall solder joint strain, thus increasing the physical reliability of lands 280.

Electrical inductance is also reduced by the presence of downbonds as is explained next. In addition to electrical contact between the back side of semiconductor device chip 100 to die attach bond pad 240, additional connections can be made from preselected device electrodes 300 as needed, by down bonding from semiconductor device chip 100 to die attach bond pad 240. Referring back to **FIG. 2**, downbonds 295 allow the preselected device electrodes of the semiconductor device chip to be electrically connected to die attach bond pad 240 and to heat spreader 290 by way of the first group of vias 255. Using downbonds 295 will also lead to minimal inductance because the length of wire used is minimal, and it thus provides for a very good electrical and thermal path from semiconductor device chip 100 to the ground plane.

The semiconductor device just described is compatible with a simple manufacturing process that comprises overmolding a plurality of devices in a panelization scheme, and then sawing the overmolded devices into single devices at the end of the manufacturing process. This allows for the semiconductor device of the present invention to make use of portions of existing manufacturing processes.

In an alternative embodiment, the bond pads 260 and lands 280 may be co-located with the vias 250. For example, **FIG. 5** illustrates a semiconductor device 120 according to that alternate embodiment of the invention. The interconnect substrate 220 may alternately be made of a ceramic material instead of a laminate material. When the interconnect substrate is made from a ceramic material, the plurality of bond pads 260 may be co-located with the second group of vias 250 on the upper surface. The plurality of lands 280 may also be co-located with the second group of vias 250 on the lower surface. This positioning of the bond pads and lands will save space, and thus will make it possible to form an electronic package that is even smaller than the previously described embodiment.

Although the present invention has been described in conjunction with particular embodiments illustrated in the appended drawing figures, various modification may be made without departing from the spirit and scope of the invention as set forth in the appended claims. For example, an alternate material may be used for the material of interconnect

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